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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,577	02/23/2004	Donald Thomas McGrath	RD-27645-2	9571

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EXAMINER	
SHINGLETON, MICHAEL B	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,577	MCGRATH, DONALD THOMAS	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-29* is/are pending in the application.

4a) Of the above claim(s) *27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26, 28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL B SHINGLETON
PRIMARY EXAMINER
ART UNIT 2817

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim 27 has been withdrawn from consideration because it is directed toward the combination of a BFL and a chopping circuit that was the subject of the previous parent application serial number 09/682,863. Note the restriction requirement in 09/682,863. The search for the combination of the BFL and the chopping circuit now present was not required for the BFL circuit. This places an additional burden on the examiner. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 27 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP 821.03.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard).

Figure 4 and the relevant text of Biard discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an "inverter stage" input "IN", a first depletion mode inverter that receives i.e. is responsive to the "inverter stage" input IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 of Biard recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Biard is also very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's)...(emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and includes depletion mode MOSFETs. Biard is silent

on the type of depletion mode MOSFET, i.e. NMOS or PMOS. NMOS and PMOS depletion mode MOSFETs are conventional forms of depletion mode MOSFETs.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used depletion mode NMOS transistors for the transistors of Biard because, as the Biard reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode FET such as the conventional depletion mode MOSFET.

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard) in further in view of Tohyama 4,810,907 (Tohyama) and Alok et al. 6,559,068 (Alok).

Figure 4 and the relevant text of Biard discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an input "IN", a first depletion mode inverter that receives the IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 of Biard recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Biard is also very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's)...(emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and includes depletion mode MOSFETs. Biard is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS. Alok discloses that silicon carbide NMOS and PMOS depletion mode MOSFETs formed on a silicon carbide substrate are conventional forms of depletion mode MOSFETs (See entire reference.). Alok also teaches the motivation for use of Silicon Carbide transistors that includes that they are ideal for "high voltage, high frequency and high temperature" (See column 1, around line 33).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used silicon carbide depletion mode NMOS transistors formed on a silicon carbide substrate for the transistors of Biard because, as the Biard reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-

recognized equivalent depletion mode FET such as the conventional silicon carbide depletion mode NMOS MOSFET formed on a silicon carbide substrate. Additionally one of ordinary skill would have been motivated to make the combination because of the higher voltage handing, the higher frequency capabilities and the higher temperature handing capabilities as compared to conventional Si based MOS devices as taught by Alok. Silicon carbide MOSFETs are better FETs.

Biard is silent on the use of resistor(s) for the voltage drop circuit.

Tohyama shows that the resistor, the diode and the "diode connected " FET like that of Biard are all art-recognized equivalent voltage drop circuits for use in BFT's.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the voltage drop circuit of Biard with a resistor because two voltage drop circuits are well known to be equivalent in the art as taught by Tohyama.

Because the combination made obvious above includes depletion mode NMOS transistors, this circuit being the same as that claimed is configured to operate with a negative direct current bias on each of the gates with respect to the associated channel.

Response to Arguments

Applicant's arguments filed 11-2-2005 have been fully considered but they are not persuasive. Applicant states that none of the references alone or in combination describe or suggest the BFL circuit of claims 26-29. The claim 27 is actually a combination claim that is the subject of the parent application and accordingly has been withdrawn from consideration. Applicant should note that if the independent claim 26 becomes allowable and all that is left in the claims are allowed claim dependent claim 27 will be checked for any 35 USC 112 issues and rejoined at this time. Examining claim 27 at this time would be examining the non-elected invention and would place an additional burden on the examiner. The remaining claims the examiner disagrees with applicant's beliefs. Claims 26, 28 and 29 are basically old claims 6, 8 and 9 with the "input" being named "an inverter stage input" instead of just "an input". Since that input stage 30 and 31 of the primary reference to Biard inverts, the input is an inverter stage input.

In addition to that above concerning claim 27, the following argument to amended claim 6-9 and 25 applies to claim 27 here. This should make it clear as to why claim 27 is directed to the non-elected invention. In response to Applicant's arguments dated 07-25-2005, Applicant argues, "if the parent application includes recitation designated as A and B, and the divisional application includes recitations designated as C and D, the amendment added a portion of B without deleting C or D. C, D, and at least a

portion of B are still independent and distinct from A and B because the divisional application still includes C and D after the amendment." However, this is not the situation here. After a restriction Applicant has filed a divisional on the subcombination B_{sp}. The parent application contained the subcombination B_{sp} directed to the buffered logic level shifting circuit (Claims 6-9 of the parent application.). The parent application also contained claims drawn to the combination AB_{br} where the combination does not set forth the details of the subcombination (Claims 1-5 and 10-24 of the parent application.). Therefore the inventions have been held as distinct. In the instant case, the parent application was not directed to A and B and the divisional to two totally different limitations C and D but the parent was originally directed to B_{sp} and AB_{br} with the subcombination being the buffered logic shifting circuit and the divisional directed to B_{sp}. "AB_{br} is an evidence claim which indicates that the combination does not rely upon the specific details of the subcombination for its patentability" (See MPEP 806.05(c) III). Now that applicant after the amendment in the instant application dated 3-11-2005 presents claims where the subcombination has disappeared and only claims directed to AB_{sp} has been presented. The issue is not what has remained the same, but what has been added and in the instant case "A" limitations has been added to the specific subcombination claims making for combination claims AB_{sp}. Note the chopper circuit. Thus the situation as presented in MPEP 806(c) III applies, namely AB_{sp}/AB_{br}(evidence claim)/B_{sp}. Note that in the MPEP 806.05(c) III that even though AB_{sp} is present, the combination was still held as distinct from the subcombination. This is the case with the amendment to the instant application. In the instant case, Applicant continues to present claim 27 that is solely directed to the combination by the inclusion of the limitations of the chopper circuit along with the subcombination subject matter, i.e. the buffered field effect transistor logic. If the newly presented claim 27 and that of the claims 6-9 and 25 of the previous amendment were originally presented in the parent application in addition to the originally filed claims in the 09/682,863 application, then these claims would be found distinct from the subcombination claims as indicated above (See MPEP 806.05(c) III). Also note that in the parent case AB_{br} was not found "unallowable" and thus there was no question of rejoinder of the inventions in the parent application. Thus AB_{sp} was considered to be distinct from the subcombination in the parent application 09/682,863 so must the AB_{sp} (Claim 27) must be considered distinct from the subcombination here in order to be consistent (See MPEP 806.05(c) III).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this

application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
January 20, 2006

Michael B Shingleton
Primary Examiner
Group Art Unit 2817